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# Input-Parallel Output-Parallel (IPOP) Three-Level (TL) DC/DC Converters with Interleaving Control Strategy for Minimizing and Balancing Capacitor Ripple Currents

Dong Liu, *Student Member, IEEE*, Fujin Deng, *Member, IEEE*, Zheng Gong, *Student Member, IEEE*, and Zhe Chen, *Senior Member, IEEE*

**Abstract**—In this paper, the input-parallel output-parallel (IPOP) three-level (TL) DC/DC converters associated with the interleaving control strategy are proposed for minimizing and balancing the capacitor ripple currents. The proposed converters consist of two four-switch half-bridge three-level (HBTL) DC/DC converters featuring with simple and compact circuit structures, which can reduce the current stresses of the components and increase the power rating of the converter. The combination of the proposed IPOP TL circuit structure and the interleaving control strategy can greatly reduce the ripple currents on the two input capacitor not only by doubling the frequencies of these ripple currents as the universal benefit of utilizing the interleaving control strategy but also by counteracting part of these ripple currents due to the operation principle of the proposed IPOP TL circuit structure. More importantly, the ripple current imbalance among the two input capacitors can be eliminated by combining the proposed IPOP TL converters and the interleaving control strategy, which can improve the converter's reliability in balancing the thermal stresses and lifetimes of the two input capacitors. The theoretical analysis of the ripple currents on the two input capacitors is presented in detail. Finally, the simulation and experimental results are presented to verify the proposed converters with the interleaving control strategy.

**Index Terms**—Input-parallel output-parallel (IPOP), ripple currents on input capacitors, three-level (TL) DC/DC converter.

## I. INTRODUCTION

DC distribution systems and DC micro-grids have been proposed as promising solutions for future smart-grid systems because of their clear merits, such as no reactive power, no frequency stability, high conversion efficiency, and easy system control [1-6]. Furthermore, DC data centers and residential systems have been increasingly developed recently [7], [8]. The performance of DC systems highly depends on

DC/DC converters, which are responsible for delivering power and changing voltage levels among DC systems. Generally, a reasonable higher DC voltage is preferred for the DC distribution systems and micro-grids to reduce the power losses and increase the power capability. Therefore, research on the high voltage and high power DC/DC converters with high performance and high reliability attracts attention [9-11].

The three-level (TL) DC/DC converter is attractive for DC distribution systems with the high DC bus voltage [12-14]. So far, a number of studies have been done on TL based DC/DC converters [15-30]. In [16], a zero-voltage and zero-current switching half-bridge three-level (HBTL) DC/DC converter was proposed, in which a flying capacitor in the primary side was added to make the phase-shift control strategy applied into TL DC/DC converter. Based on [16], an auxiliary circuit was added in the secondary side to reduce the circulating current for improving the efficiency [17]. In [18], a new zero-voltage switching (ZVS) four-switch HBTL DC/DC converter was proposed, which featured with simple and compact circuit structure by adding one additional wire between the mid-points of the input capacitors and switching pairs but removing two clamped diodes. In [19], a FB DC/DC converter combined by a HBTL DC/DC converter and a HB two-level DC/DC converter was proposed for high power applications. Two kinds of control strategies for an isolated FB TL DC/DC converter were presented in [20] and [21], respectively, in which a double phase-shift control strategy was proposed to achieve soft switching in FB TL converter and a novel modulation strategy was proposed for reducing the voltage stress on the transformer and balancing the voltage of two input capacitors. Recently, hybrid TL DC/DC converters, which combined two or more topologies by sharing some switches, have been presented to improve the efficiency or minimize the size of the filter inductor [22-26]. Two TL DC/DC converters, which were hybrid with LLC converter and half-bridge converter, were presented in [27] and [28] to reduce the circulating current and extend ZVS range. In addition, a secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain was proposed in [29], which not only can reduce the switching losses by realizing ZVS but also can minimize the conduction losses by suppressing the

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circulating current at the freewheeling stage.

The above studies mainly focus on the topics about soft switching techniques, power density and the efficiency of the converter. Unfortunately, few studies pay attentions on the ripple currents on the input capacitors in the TL based DC/DC converters, which affect the reliability of the converter [31], [32]. In reference [18], it is analyzed that two ripple currents among the two input capacitors in the four-switch HBTL DC/DC converter are balanced based on the assumption that the input power supply is regarded as an ideal voltage source, which means that the input current can change abruptly along with the switching actions. However, in the real applications, the abrupt changes of the input current in the switching period are impractical due to the effect from the output inductance of the input power supply and the inductance of the input line on the input current, which would result in the ripple current imbalance among the two input capacitors.

In addition, the four-switch HBTL DC/DC converter is a half-bridge topology, which is not suitable for the high power applications comparing with the full-bridge topology. Connecting modular converters with input-parallel and output-parallel (IPOP) is an efficient and reliable method to increase the power rating of the converters for high power applications [33-36]. Reference [35] proposed a parallel inductive power transfer topology to achieve high output power. In [36], a common-duty-ratio scheme based interleaving control strategy was proposed, which can share the input and output currents among the two modules automatically.

In this paper, the IPOP TL DC/DC converters associated with the interleaving control strategy are proposed to minimize and balance the ripple currents through the two input capacitors. The proposed converters are composed of two four-switch HB TL DC/DC converters featuring with simple and compact circuit structure, which can reduce the current stresses of the power switches, the transformers, and the output filters. The combination of the proposed IPOP TL circuit structure and the interleaving control strategy not only can double the frequencies of these ripple currents as the universal benefit of using the interleaving control strategy, but also can counteract part of these ripple currents due to the operation principle of the proposed circuit structure, which thus can largely reduce the ripple currents on the two input capacitors. What is more, the ripple currents through the two input capacitors can be kept almost the same by combining the proposed converters and the interleaving control strategy. Consequently, the proposed converters with the interleaving control strategy can minimize the input capacitors' sizes, balance the input capacitors' thermal stresses, prolong the input capacitors' lifetimes, and thus improve the converter's performance and reliability.

This paper is organized as follows. Section II introduces the circuit structure of the proposed converters and analyzes the operation principle of the proposed converters in detail. Section III analyzes the performances of the proposed converters with the interleaving control strategy, especially for the capacitor ripple currents, and compares some of these performances with that without the interleaving control

strategy. Section IV presents the simulation and experimental results to verify the effectiveness and feasibility of the proposed converters associated with the interleaving control strategy. Finally, the main contributions of this paper are summarized in Section V.

## II. CIRCUIT STRUCTURE AND OPERATION PRINCIPLE

Fig. 1 shows the circuit structure of the proposed IPOP TL DC/DC converters, which is composed of two four-switch HB TL DC/DC converters namely module-1 and module-2. There are two sharing input capacitors  $C_1$  and  $C_2$  used to split the input voltage  $V_{in}$  into two voltages  $V_1$  and  $V_2$  and one sharing output filter capacitor  $C_o$  as shown in Fig. 1. In the module-1,  $S_1$ - $S_4$  and  $D_1$ - $D_4$  are power switches and diodes;  $T_{r1}$  is the high frequency transformer;  $L_{r1}$  is the leakage inductance of  $T_{r1}$ ;  $C_{b1}$  is the DC-blocking capacitor;  $D_{r1}$ - $D_{r4}$  are output rectifier diodes;  $L_{o1}$  is the output filter inductor. The circuit structure of the module-2 is the same as that of the module-1, in which  $S_5$ - $S_8$  and  $D_5$ - $D_8$  are power switches and diodes;  $T_{r2}$  is the high frequency transformer;  $L_{r2}$  is the leakage inductance of  $T_{r2}$ ;  $C_{b2}$  is the DC-blocking capacitor;  $D_{r5}$ - $D_{r8}$  are output rectifier diodes;  $L_{o2}$  is the output filter inductor. In Fig. 1,  $i_{in}$  is the input current;  $i_{c1}$  and  $i_{c2}$  are currents on  $C_1$  and  $C_2$ , respectively;  $i_{p1}$  and  $i_{p2}$  are primary currents of  $T_{r1}$  and  $T_{r2}$ ;  $i_{L_{o1}}$  and  $i_{L_{o2}}$  are currents through  $L_{o1}$  and  $L_{o2}$ ;  $V_{cb1}$  and  $V_{cb2}$  are voltages on  $C_{b1}$  and  $C_{b2}$ ;  $i_o$  and  $V_o$  are the output current and output voltage;  $V_{ab}$  is the voltage between point a and b;  $V_{cd}$  is the voltage between point c and d;  $n_1$  and  $n_2$  are turns ratios of  $T_{r1}$  and  $T_{r2}$ .

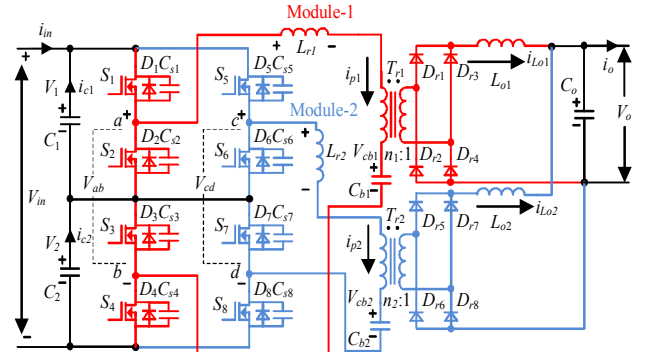


Fig. 1. Circuit structure of the proposed IPOP TL DC/DC converters.

Before discussing the operation principle of the proposed converters, some assumptions are made as below:

- 1) The output filter inductors  $L_{o1}$  and  $L_{o2}$  are the same and large enough to be considered as the current sources;
- 2) The switches  $S_1$ - $S_8$  are ideal, which means the effects of the switch parasitic capacitors are neglected;
- 3)  $C_1$ ,  $C_2$ ,  $C_{b1}$ , and  $C_{b2}$  are large enough to be considered as voltage sources and  $C_1 = C_2 = C_{in}$ ,  $C_{b1} = C_{b2} = C_b$ ,  $V_1 = V_2 = V_{in}/2$ ,  $V_{cb1} = V_{cb2} = V_{cb} = V_{in}/2$ ;
- 4) The parameters of the two transformers  $T_{r1}$  and  $T_{r2}$  are identical, having the same turns ratios  $n_1 = n_2 = n$  and the same leakage inductances  $L_{r1} = L_{r2} = L_r$ ;
- 5) The input current  $i_{in}$  is considered as a constant in the switching period due to the effect from the output inductance of the input power supply and inductance of the input line on the input current.

Fig. 2(a) and (b) show the operation principle of the proposed converters without and with the interleaving control strategy, respectively. In Fig. 2,  $d_{rv1}$ - $d_{rv8}$  are eight driving signals of the power switches  $S_1$ - $S_8$ ,  $d_1$ - $d_2$  are duty ratios in one switching period,  $T_s$  is the time of one switching period, and  $(S_1, S_2)$ ,  $(S_3, S_4)$ ,  $(S_5, S_6)$ , and  $(S_7, S_8)$  are complementary switch pairs. Without the interleaving control strategy,  $(S_1, S_5)$ ,  $(S_2, S_6)$ ,  $(S_3, S_7)$ , and  $(S_4, S_8)$  are switch pairs having the same driving signal as shown in Fig. 2(a). Contrarily,  $(S_1, S_7)$ ,  $(S_2, S_8)$ ,  $(S_3, S_5)$ , and  $(S_4, S_6)$  are switch pairs having the same driving signal with the interleaving control strategy as shown in Fig. 2(b). In Fig. 2, the output voltages with and without the interleaving control strategy are both adjusted by changing the duty ratio  $d_1$ , and  $d_2 = 1 - d_1$  if neglecting the dead-time. As plotted by red color in Fig. 2(a), the ripple currents among the two input capacitors are imbalance when the proposed converters operate without the interleaving control strategy. Contrarily, with the interleaving control strategy, the ripple currents  $i_{c1}$  and  $i_{c2}$  are kept the same and much smaller than that without the interleaving control strategy as figured by red color in Fig. 2(b). One thing that needs to be mentioned is that the ripple current  $i_{c1}$  without the interleaving control strategy during some time periods, as highlighted in Fig. 2(a), would be greatly reduced after utilizing the interleaving control strategy as highlighted in Fig. 2(b) because part of the ripple current  $i_{c1}$  can be counteracted during these time periods, which will be explained in detail below.

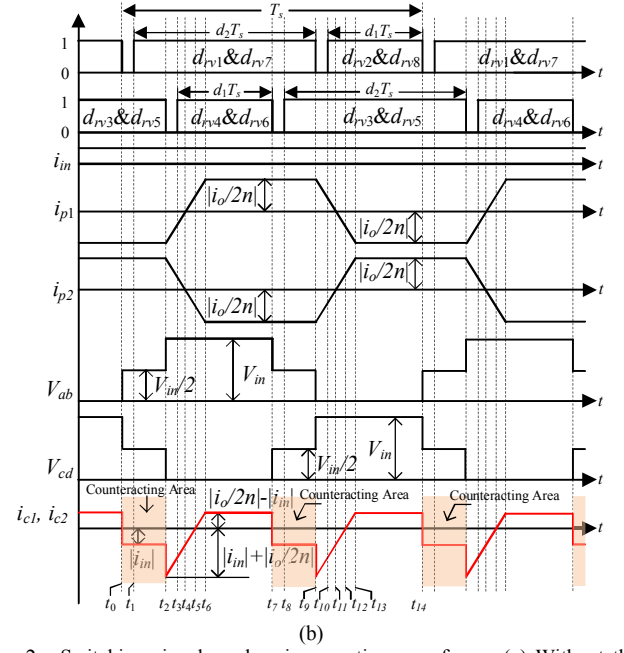
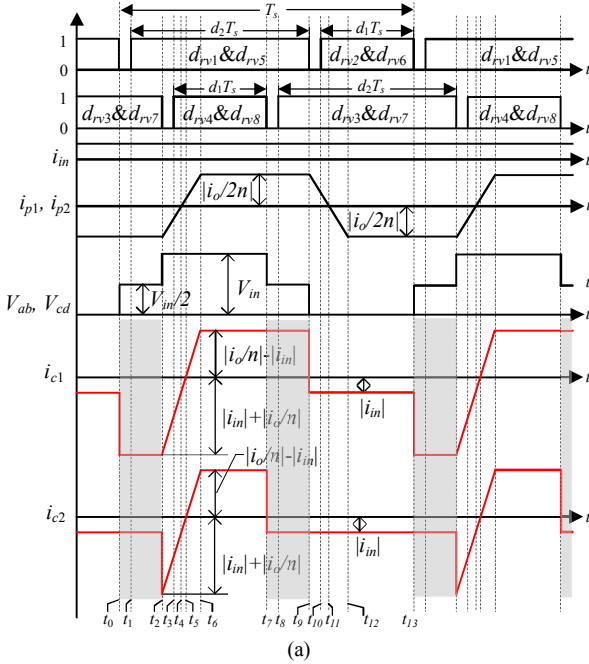


Fig. 2. Switching signals and main operation waveforms. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

Fig. 3 shows the equivalent circuits to explain the operation principle of the proposed converters associated with the interleaving control strategy shown in Fig. 2(b).

Stage 1  $[t_0-t_1]$ : At  $t_0$ , switches  $S_2$  and  $S_8$  are turned off.  $V_{ab}$  increases to  $V_{in}/2$  and  $V_{cd}$  decreases to  $V_{in}/2$ . The currents  $i_{p1}$  and  $i_{p2}$  would only freewheel through  $D_1, S_5, L_{r2}, T_{r2}, C_{b2}, D_7, S_3, C_{b1}, T_{r1}$ , and  $L_{r1}$  but not flow through  $C_1$ , which means the  $i_{p1}$  through  $C_1$  and  $i_{p2}$  through  $C_1$  counteract each other, as highlighted in Fig. 2(b). Therefore, during this stage,  $i_{c1}$  and  $i_{c2}$  are the same, which are both  $-i_{in}$ .

Stage 2  $[t_1-t_2]$ : At  $t_1$ , switches  $S_1$  and  $S_7$  are turned on at zero-voltage. The currents  $i_{p1}$  and  $i_{p2}$  would freewheel through  $S_1, S_5, L_{r2}, T_{r2}, C_{b2}, S_7, S_3, C_{b1}, T_{r1}$ , and  $L_{r1}$ , which means the  $i_{p1}$  through  $C_1$  and  $i_{p2}$  through  $C_1$  still counteract each other, as highlighted in Fig. 2(b). Therefore, these switching actions have no effect on  $i_{c1}$  and  $i_{c2}$  whose values maintain  $-i_{in}$ .

Stage 3  $[t_2-t_3]$ : At  $t_2$ , the switches  $S_3$  and  $S_5$  are turned off. The current  $i_{p1}$  would freewheel through  $S_1, C_1, C_2$ , and  $D_4$ .  $V_{ab}$  increases to  $V_{in}$ , therefore  $i_{p1}$  starts to increase linearly. The current  $i_{p2}$  would freewheel through  $S_7$  and  $D_6$ .  $V_{cd}$  decreases to 0 V, therefore  $i_{p2}$  begins to decrease linearly. The expressions of  $i_{p1}$  and  $i_{p2}$  are

$$i_{p1} = -\frac{i_o}{2 \cdot n} + \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) \quad (1)$$

$$i_{p2} = \frac{i_o}{2 \cdot n} - \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) \quad (2)$$

The currents  $i_{c1}$  and  $i_{c2}$  change to  $-(|i_{in}| + |i_{p1}|)$  from  $-i_{in}$  and start to increase. During this stage, output rectifier diodes  $D_{r1}$ - $D_{r4}$  and  $D_{r5}$ - $D_{r8}$  turn on simultaneously, therefore there is no power transferring from the input power and  $C_{b1}$  to the output.

Stage 4  $[t_3-t_4]$ : At  $t_3$ , switches  $S_4$  and  $S_6$  are turned on at zero-voltage. The current  $i_{p1}$  would freewheel through  $S_1, C_1, C_2$ , and  $S_4$ . The voltage of  $V_{ab}$  remains  $V_{in}$ . The current  $i_{p2}$

would freewheel through  $S_7$  and  $S_6$ . The voltage of  $V_{cd}$  still equals to 0 V. During this stage,  $i_{c1}$  and  $i_{c2}$  are still increasing and their absolute values stay at  $|i_{in}| + |i_{p1}|$ .

Stage 5 [ $t_4$ - $t_5$ ]: At  $t_4$ ,  $i_{p1}$  increases to 0 A and  $i_{p2}$  decreases to 0 A, then current directions of  $i_{p1}$  and  $i_{p2}$  begin to change, the absolute value of  $i_{c1}$  and  $i_{c2}$  change to  $|i_{in}| - |i_{p1}|$ .

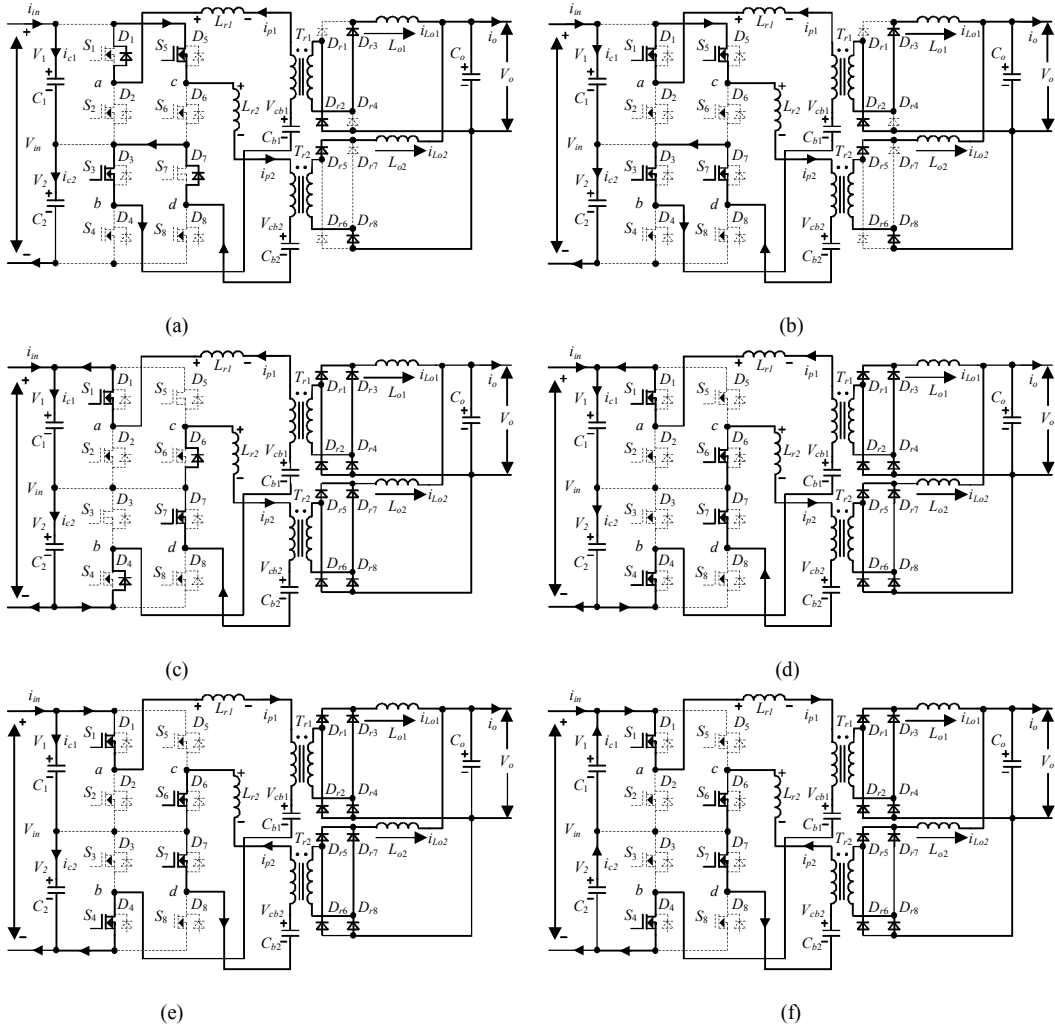
Stage 6 [ $t_5$ - $t_6$ ]: At  $t_5$ , the currents  $i_{c1}$  and  $i_{c2}$  increase to 0 A, then the current directions of  $i_{c1}$  and  $i_{c2}$  begin to change, the absolute value of  $i_{c1}$  and  $i_{c2}$  change to  $|i_{p1}| - |i_{in}|$ .

Stage 7 [ $t_6$ - $t_7$ ]: At  $t_6$ , the current  $i_{p1}$  reaches to  $i_o/2n$ , and then the input power begins to be transferred to output through  $T_{r1}$ ,  $D_{r1}$ , and  $D_{r4}$ . The current  $i_{p2}$  decreases to  $-i_o/2n$ , and then the power from  $C_{b2}$  begins to transfer to output through  $T_{r2}$ ,  $D_{r6}$ , and  $D_{r7}$ .  $i_{p1}$  and  $i_{p2}$  are kept at  $i_o/2n$  and  $-i_o/2n$ . During this period, the absolute value of  $i_{c1}$  and  $i_{c2}$  remain  $|i_{p1}| - |i_{in}|$ .

The analysis of the second half switching period [ $t_7$ - $t_{14}$ ] is similar to the first half period [ $t_0$ - $t_7$ ], which is not repeated

here. At  $t_{14}$ , the following operation in next period starts, which is the same as the first switching period.

Based on the above operation principle analysis about the combination of the proposed IPOP TL converters and the interleaving control strategy, it can be concluded that: 1) the frequencies of  $i_{c1}$  and  $i_{c2}$  are twice of the switching frequency because of utilizing the interleaving control strategy, which can reduce the currents on the two input capacitors  $i_{c1}$  and  $i_{c2}$ ; 2) part of the ripple current  $i_{c1}$  can be counteracted as highlighted time periods in Fig. 2(b) because the primary currents of the two modules  $i_{p1}$  and  $i_{p2}$  flowing through the input capacitor  $C_1$  would counteract each other during these highlighted time periods, which is illustrated in the above principle analysis of Stage 1 and Stage 2; 3) based on the benefits of (1) and (2), the ripple currents  $i_{c1}$  and  $i_{c2}$  can be largely reduced and kept the same.



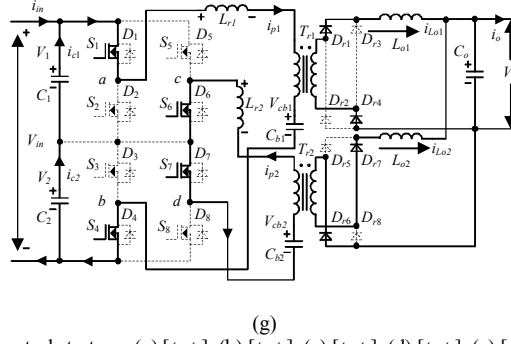


Fig. 3. Equivalent circuits with the interleaving control strategy. (a)  $[t_0-t_1]$ . (b)  $[t_1-t_2]$ . (c)  $[t_2-t_3]$ . (d)  $[t_3-t_4]$ . (e)  $[t_4-t_5]$ . (f)  $[t_5-t_6]$ . (g)  $[t_6-t_7]$ .

### III. PERFORMANCES OF THE PROPOSED CONVERTERS

In this section, the performances of the proposed converters associated with the interleaving control strategy are analyzed in detail.

#### A. Voltages and Currents of Power Switches

Due to the TL structure, all the power switches of the proposed IPOP TL converters only need to withstand half of the input voltage ( $V_{in}/2$ ) in the steady operation. In addition, the currents  $i_{p1}$  and  $i_{p2}$  would flow through the power switches in the proposed converters, so the theoretical maximum current of the power switches is  $i_o/2n$  in the steady operation.

#### B. Output Characteristic

The voltages on the two DC-blocking capacitors in the steady operations are

$$V_{cb1} = V_{cb2} = V_{cb} = \frac{V_{in}}{2} \quad (3)$$

If temporarily neglect the duty ratio loss, the output voltage  $V_o$  is

$$V_o = \frac{1}{n} \cdot [(V_{in} - V_{cb}) \cdot d_1 + V_{cb} \cdot d_1] \quad (4)$$

Substituting (4) into (3), the output voltage  $V_o$  can be rewritten as

$$V_o = \frac{V_{in}}{n} \cdot d_1 \quad (5)$$

According to Fig. 2(b), the duty cycle losses in one switching period can be described as

$$d_{loss1} = d_{loss2} = d_{loss} = 2 \cdot \left( \frac{t_6 - t_2}{T_s} \right) = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \quad (6)$$

where  $d_{loss1}$  and  $d_{loss2}$  are the duty cycle losses of the two four-switch HBTL converters.

If considering the effect of duty cycle loss on the output voltage,  $V_o$  can be further calculated as (7) based on (5) and (6).

$$V_o = \frac{V_{in}}{n} \cdot \left( d_1 - \frac{d_{loss}}{2} \right) = \frac{V_{in}}{n} \cdot \left( d_1 - \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \right) \quad (7)$$

#### C. Ripple Voltages on DC-blocking Capacitors

According to Fig. 2(b), if neglecting the effect of the duty cycle loss, both  $C_{b1}$  and  $C_{b2}$  are charged in  $T_s/2$  and discharged in  $T_s/2$  by the current  $i_o/2n$ . Therefore, the ripple voltages on

$C_{b1}$  and  $C_{b2}$  can be calculated by

$$\Delta V_{cb1} = \Delta V_{cb2} = \frac{\frac{i_o}{2n} \cdot \frac{T_s}{2}}{C_b} = \frac{i_o \cdot T_s}{4 \cdot n \cdot C_b} \quad (8)$$

where  $\Delta V_{cb1}$  and  $\Delta V_{cb2}$  are the ripple voltages on  $C_{b1}$  and  $C_{b2}$ , respectively.

#### D. Ripple Currents on Two Input Capacitors

According to the analysis in the Section II,  $i_{c1}$  and  $i_{c2}$  in a half switching period, as shown in Fig. 2(b), can be expressed as

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ i_{p1} - i_{in} & t_2 \leq t < t_7 \end{cases} \quad (9)$$

The currents  $i_{p1}$  and  $i_{p2}$  are opposite as shown in Fig. 2(b), whose expressions in a half switching period can be given by

$$i_{p1} = -i_{p2} = \begin{cases} -\frac{i_o}{2 \cdot n} & t_0 \leq t < t_2 \\ -\frac{i_o}{2 \cdot n} + \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & t_2 \leq t < t_6 \\ \frac{i_o}{2 \cdot n} & t_6 \leq t < t_7 \end{cases} \quad (10)$$

Substituting (10) into (9),  $i_{c1}$  and  $i_{c2}$  in half switching period can be rewritten by

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{2 \cdot n} - i_{in} & t_2 \leq t < t_6 \\ \frac{i_o}{2 \cdot n} - i_{in} & t_6 \leq t < t_7 \end{cases} \quad (11)$$

The time intervals  $[t_2-t_6]$  and  $[t_9-t_{13}]$  are the same as shown in Fig. 2(b), which can be obtained by

$$t_6 - t_2 = t_{13} - t_9 = \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in}} \quad (12)$$

According to (11) and (12), the root mean square (RMS) values of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy namely  $i_{c1\_rms\_II}$  and  $i_{c2\_rms\_II}$  can be calculated by (13), which is listed in the Table I.

Similar to the above analysis, the RMS values of  $i_{c1}$  and  $i_{c2}$  without the interleaving control strategy as shown in Fig. 2(a) namely  $i_{c1\_rms\_I}$  and  $i_{c2\_rms\_I}$  can be calculated by (14) and (15), which are listed in the Table I.

Based on (14) and (15), the difference between  $i_{c1\_rms\_I}$  and  $i_{c2\_rms\_I}$  namely  $\Delta i_{c\_rms\_I}$  can be calculated by (16), which is

$$i_{c1\_rms\_II} = i_{c2\_rms\_II} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{2 \cdot n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{2 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (13)$$

$$i_{c1\_rms\_I} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_2}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (14)$$

$$i_{c2\_rms\_I} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (15)$$

$$\Delta i_{c\_rms\_I} = i_{c1\_rms\_I} - i_{c2\_rms\_I} = \frac{i_o^2 \cdot (d_2 - d_1)}{n^2 \cdot (i_{c1\_rms\_I} + i_{c2\_rms\_I})} \quad (16)$$

Table I shows that: First, the RMS values of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy are smaller than that without the interleaving control strategy because: 1) the second items in the formulas of  $i_{c1\_rms\_II}$  and  $i_{c2\_rms\_II}$  are half of that in the formula of  $i_{c2\_rms\_I}$ ; and 2) the value of  $L_r$  is small so that its effect on the fifth items in the formulas of  $i_{c1\_rms\_I}$ ,  $i_{c2\_rms\_I}$ ,  $i_{c1\_rms\_II}$ , and  $i_{c2\_rms\_II}$  can be negligible normally. Second,  $i_{c1\_rms\_I}$  and  $i_{c2\_rms\_I}$  are different and  $i_{c1\_rms\_I}$  is bigger than  $i_{c2\_rms\_I}$  because  $d_2$  is bigger than  $d_1$  in normal operations, but

$i_{c1\_rms\_II}$  and  $i_{c2\_rms\_II}$  are the same, which means the ripple current imbalance among the two input capacitors is eliminated by combining the proposed IPOP TL circuit structure and the interleaving control strategy. The operational principle and main operation waveforms without the interleaving control strategy in the proposed converters are similar to that in the four-switch HBTL DC/DC converter, which means that the ripple current imbalance issue also exists in the four-switch HBTL DC/DC converter.

TABLE I  
THEORETICAL CALCULATION FORMULAS OF RMS VALUES OF  $i_{c1}$  AND  $i_{c2}$

Control Strategy	RMS Value	Theoretical Calculation Formula
Without the interleaving control strategy	$i_{c1\_rms\_I}$	$\sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_2}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$i_{c2\_rms\_I}$	$\sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{4 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$\Delta i_{c\_rms\_I}$	$\frac{i_o^2 \cdot (d_2 - d_1)}{n^2 \cdot (i_{c1\_rms\_I} + i_{c2\_rms\_I})}$
With the interleaving control strategy	$i_{c1\_rms\_II}, i_{c2\_rms\_II}$	$\sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{2 \cdot n^2} + \frac{4 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{2 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$

Through applying the circuit parameters in the Appendix into the theoretical calculation formulas in the Table I, the theoretical calculation results about the RMS values of  $i_{c1}$  and  $i_{c2}$  with various input voltages and output power are shown in Fig. 4, where the output voltage is 50 V.

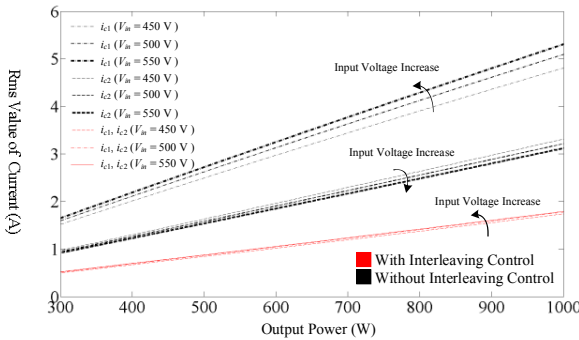


Fig. 4. RMS values of  $i_{c1}$  and  $i_{c2}$  with various input voltages and output power.

Fig. 4 shows that: 1) the RMS values of  $i_{c1}$  and  $i_{c2}$  without the interleaving control strategy are different and the RMS value of  $i_{c1}$  is bigger than that of  $i_{c2}$ , but the RMS values of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy are the same; 2) the RMS values of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy are much smaller than that without the interleaving control strategy. From Fig. 4, it can be also observed that: 1) the difference between the RMS values of  $i_{c1}$  and  $i_{c2}$  without the interleaving control strategy ( $\Delta i_{c\_rms\_I}$ ) increases with the output power increasing; 2) the difference between the RMS values of  $i_{c1}$  and  $i_{c2}$  without the interleaving control strategy increases with the input voltage increasing since the RMS value of  $i_{c2}$  decreases but the RMS value of  $i_{c1}$  increases with the input voltage increasing; 3) the RMS values of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy have very small changes with the input voltage increasing because the combination of the proposed IPOP TL converters and the interleaving control strategy can counteract part of these ripple currents. In Fig. 4,



the difference between the RMS values of  $i_{c1}$  and  $i_{c2}$  without the interleaving control strategy ( $\Delta i_{c\_rms\_I}$ ) reaches 2.2 A when the input voltage increases to 550 V and the output power increases to 1-kW.

#### E. Ripple Voltages on Two Input Capacitors

According to Fig. 2(b) and (9), the currents  $i_{c1}$  and  $i_{c2}$  can be further expressed as

$$i_{c1} = i_{c2} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{2 \cdot n} - i_{in} & t_2 \leq t < t_5 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_5) & t_5 \leq t < t_6 \\ \frac{i_o}{2 \cdot n} - i_{in} & t_6 \leq t < t_7 \end{cases} \quad (17)$$

The input capacitors  $C_1$  and  $C_2$  are discharged in the time period  $[t_0-t_5]$  and charged in the time period  $[t_5-t_7]$  as shown in Fig. 2(b). These time intervals in Fig. 2(b) can be obtained by

$$\Delta V_{1\_II} = \Delta V_{2\_II} = \frac{i_{in} \cdot \left(\frac{d_2 - d_1}{2}\right) \cdot T_s + \frac{L_r \cdot i_o^2}{4 \cdot n^2 \cdot V_{in}} + \frac{L_r \cdot i_{in} \cdot i_o}{n \cdot V_{in}} + \frac{L_r \cdot i_{in}^2}{V_{in}}}{C_{in}} \quad (19)$$

$$\Delta V_{1\_I} = \frac{\left(\frac{i_o}{2 \cdot n} + i_{in}\right) \cdot (d_2 - d_1) \cdot T_s + \frac{L_r \cdot i_o^2}{2 \cdot n^2 \cdot V_{in}} + \frac{L_r \cdot i_{in} \cdot i_o}{n \cdot V_{in}} + \frac{L_r \cdot i_{in}^2}{2 \cdot V_{in}}}{C_1} \quad (20)$$

$$\Delta V_{2\_I} = \frac{i_{in} \cdot d_2 \cdot T_s + \frac{L_r \cdot i_o^2}{2 \cdot n^2 \cdot V_{in}} + \frac{L_r \cdot i_{in} \cdot i_o}{n \cdot V_{in}} + \frac{L_r \cdot i_{in}^2}{2 \cdot V_{in}}}{C_2} \quad (21)$$

By applying the circuit parameters in the Appendix into (19)-(21), the theoretical calculation results about  $\Delta V_1$  and  $\Delta V_2$  with various output power are illustrated in Fig. 5 under the working conditions that the input voltage is 550 V and the output voltage is 50 V.

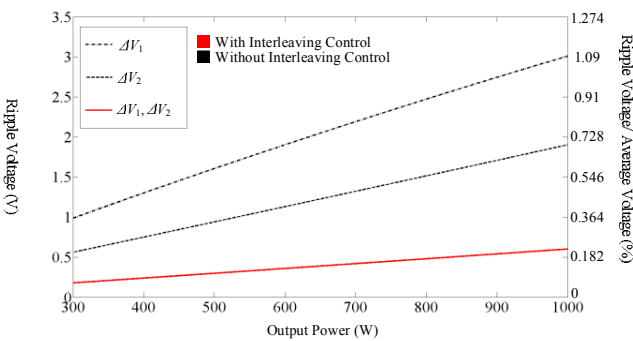


Fig. 5. Ripple voltages on the two input capacitors  $C_1$  and  $C_2$  with various output power ( $V_{in} = 550$  V,  $V_o = 50$  V). Note that the average voltages on the two input capacitors are both 275 V.

Fig. 5 shows that: 1)  $\Delta V_1$  and  $\Delta V_2$  with the interleaving control strategy are much smaller than  $\Delta V_1$  and  $\Delta V_2$  without the interleaving control strategy, which means that the input capacitor size with the interleaving control strategy can be minimized because the capacitances of the input capacitors with the interleaving control strategy would be much smaller

$$\begin{cases} t_2 - t_0 = \frac{d_2 - d_1}{2} \cdot T_s \\ t_5 - t_2 = \frac{L_r \cdot i_o}{n \cdot V_{in}} + \frac{2 \cdot L_r \cdot i_{in}}{V_{in}} \\ t_6 - t_5 = \frac{L_r \cdot i_o}{n \cdot V_{in}} - \frac{2 \cdot L_r \cdot i_{in}}{V_{in}} \\ t_7 - t_6 = d_1 \cdot T_s - \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in}} \end{cases} \quad (18)$$

Based on (17) and (18), the ripple voltages  $\Delta V_{1\_II}$  and  $\Delta V_{2\_II}$  on the input capacitors  $C_1$  and  $C_2$ , respectively, with the interleaving control strategy can be calculated by (19) in the steady operations.

Similar to the above analysis, the ripple voltages  $\Delta V_{1\_I}$  and  $\Delta V_{2\_I}$  on the input capacitors  $C_1$  and  $C_2$ , respectively, without the interleaving control strategy can be calculated by (20) and (21) in the steady operations.

than that without the interleaving control strategy if the requirements of the ripple voltages on the input capacitors are the same; 2)  $\Delta V_1$  and  $\Delta V_2$  without the interleaving control strategy are different and  $\Delta V_1$  is bigger than  $\Delta V_2$ , but  $\Delta V_1$  and  $\Delta V_2$  with the interleaving control strategy are the same; 3) with the output power increasing, the difference between  $\Delta V_1$  and  $\Delta V_2$  without the interleaving control strategy becomes larger.

## IV. SIMULATION AND EXPERIMENTAL VERIFICATION

### A. Simulation Verification

In order to validate the effectiveness and feasibility of the proposed IPOPTL converters associated with the interleaving control strategy, a simulation model is built in PLECS, whose circuit parameters are listed in the Appendix. In the simulation, the input voltage is 550 V, the output voltage is 50 V, and the output power is 1-kW.

Fig. 6 shows the simulation results, in which it can be seen that the frequencies of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy are twice of that without the interleaving control strategy. In addition,  $i_{c1}$  and  $i_{c2}$  are different without the interleaving control strategy, whose RMS values are 5.8 A and 3.2 A respectively, as shown in Fig. 6(a). On the contrary, after utilizing the interleaving control strategy,  $i_{c1}$  and  $i_{c2}$  become the same and their RMS values reduce to both 1.76 A



as shown in Fig. 6(b). In summary, the simulation results verify that the ripple currents on  $C_1$  and  $C_2$  are greatly reduced and effectively balanced due to the combination of the proposed IPOP TL circuit structure and the interleaving control strategy.

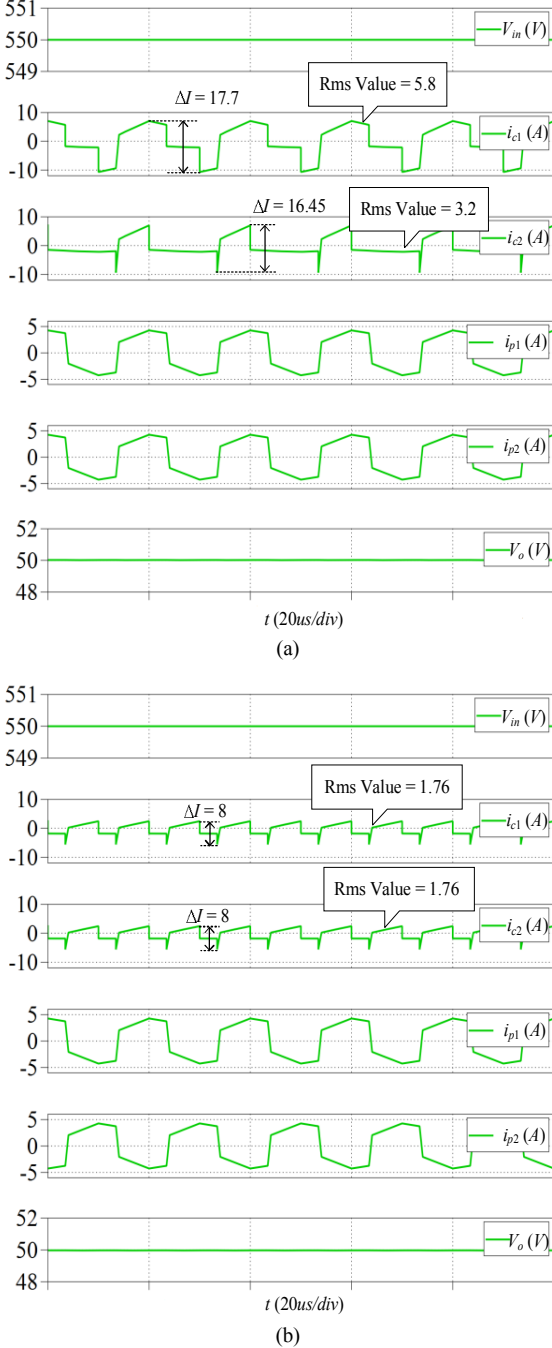


Fig. 6. Simulation results. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

### B. Experimental Verification

A 1-kW 50 kHz prototype is established to verify the above theoretical analysis. The circuit specifications of the prototype are listed in the Appendix. The input voltage is 450 V ~ 550 V, and the output voltage is 50 V. The transformer turns ratios of  $T_{r1}$  and  $T_{r2}$  are both 38:13. In the built prototype,

SPW47N60C3 is adopted as the primary power switches and MBR20200CTG is selected for the output rectifier diodes. Fig. 7 presents the built prototype used for the test.

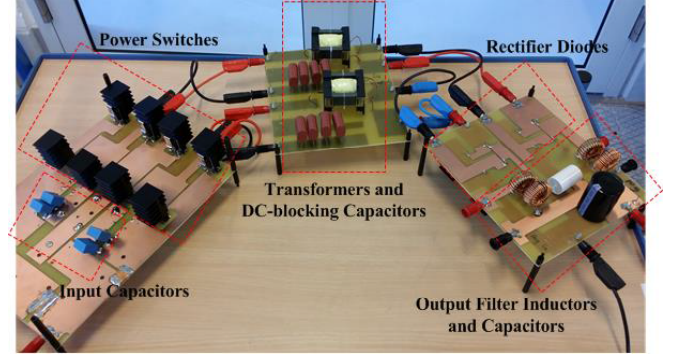


Fig. 7. 1-kW prototype of the proposed IPOP TL DC/DC converters.

Figs. 8 - 11 show the performances of the established prototype under the two operation conditions. Figs. 8 and 9 show the performances of the established prototype under the operation condition that the input voltage  $V_{in}$  is 550 V, the output voltage  $V_o$  is 50 V, and the output power is 500 W. Figs. 8(a) and (b) show the currents  $i_{p1}$ ,  $i_{p2}$  and voltages  $V_{in}$ ,  $V_o$  without and with the interleaving control strategy, respectively. In Fig. 8,  $i_{p1}$  and  $i_{p2}$  are almost the same without the interleaving control strategy, but  $i_{p1}$  and  $i_{p2}$  are opposite with the interleaving control strategy. In Fig. 9(a),  $i_{c1}$  and  $i_{c2}$  are different without the interleaving control strategy, whose RMS values are 3.2 A and 1.68 A respectively, so the difference between them are 1.52 A. Contrarily,  $i_{c1}$  and  $i_{c2}$  are almost the same with the interleaving control strategy and their RMS values decrease to 0.978 A and 0.971 A, respectively, as shown in Fig. 9(b).

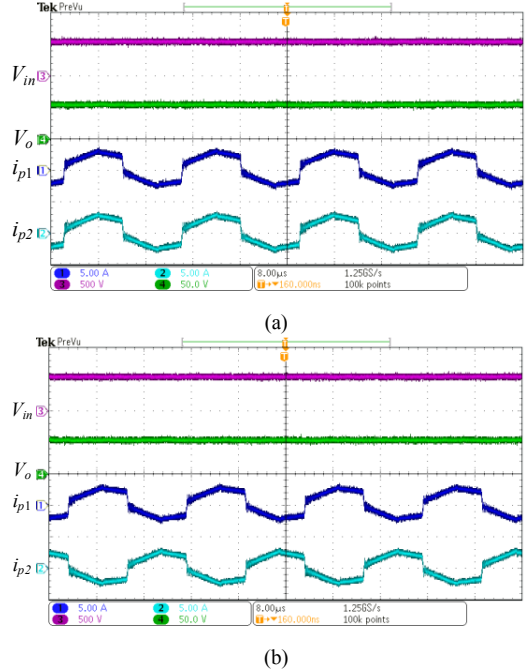


Fig. 8. Experimental results including  $V_{in}$ ,  $V_o$ ,  $i_{p1}$ , and  $i_{p2}$  under 500 W. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

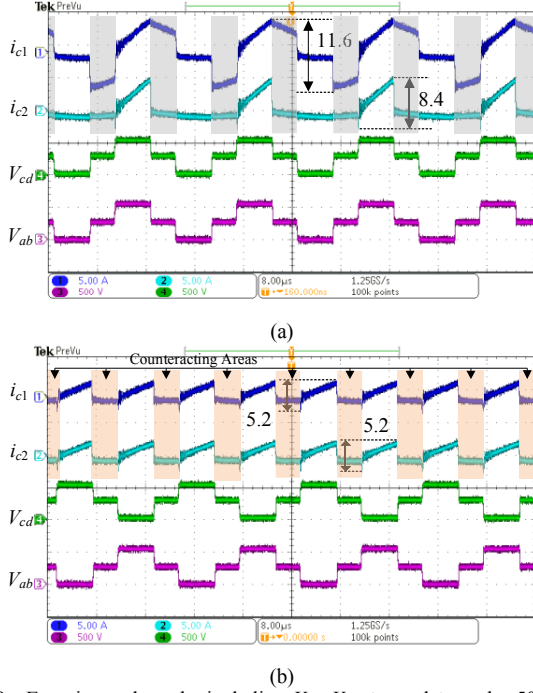


Fig. 9. Experimental results including  $V_{ab}$ ,  $V_{cd}$ ,  $i_{c1}$ , and  $i_{c2}$  under 500 W. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

Figs. 10 and 11 show the performances of the established prototype under the operation condition that the input voltage  $V_{in}$  is 550 V, the output voltage  $V_o$  is 50 V, and the output power is 1-kW. Without the interleaving control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are 5.6 A and 3.19 A as shown in Fig. 11(a), so the difference between them is 2.41 A. With the interleaving control strategy,  $i_{c1}$  and  $i_{c2}$  become almost the same and their RMS values reduce to 1.69 A and 1.68 A, respectively, as shown in Fig. 11(b).

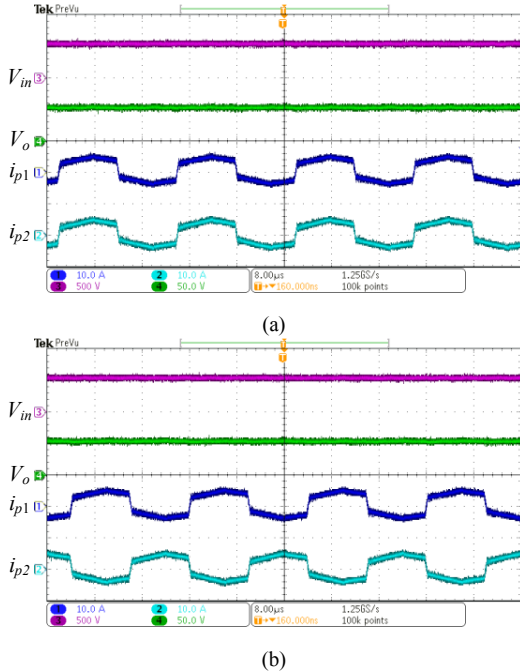


Fig. 10. Experimental results including  $V_{in}$ ,  $V_o$ ,  $i_{p1}$ , and  $i_{p2}$  under 1-kW. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

strategy.

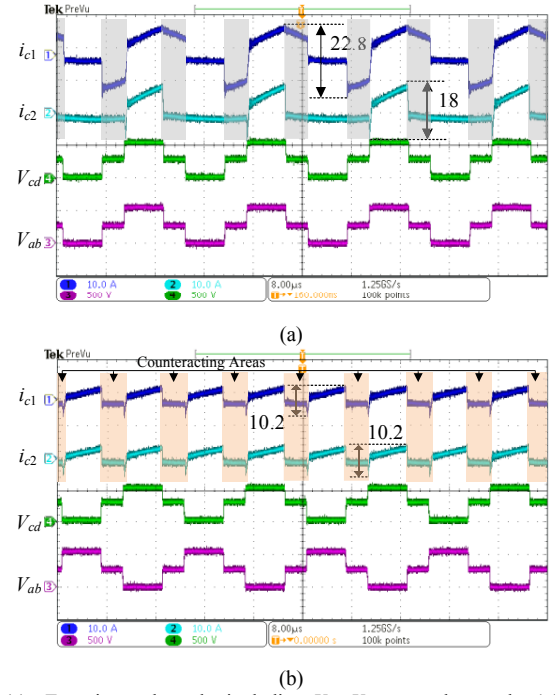


Fig. 11. Experimental results including  $V_{ab}$ ,  $V_{cd}$ ,  $i_{c1}$ , and  $i_{c2}$  under 1-kW. (a) Without the interleaving control strategy. (b) With the interleaving control strategy.

Based on the experimental results in Figs. 9 and 11, it can be observed that: 1) the frequencies of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy are twice of that without the interleaving control strategy, which is the universal benefit of using the interleaving control strategy; 2) through comparing between the results with and without the interleaving control strategy as highlighted in Figs. 9 and 11, part of the ripple current  $i_{c1}$  can be counteracted during some time periods due to combining the proposed circuit structure and interleaving control strategy as highlighted in Figs. 9(b) and 11(b), which is consistent with the operation principle analysis in the Section II; 3) due to the benefits of (1) and (2), the ripple currents on the two input capacitor can be largely reduced and kept almost the same.

Fig. 12 shows the theoretical calculation and experimental results about the RMS values of  $i_{c1}$  and  $i_{c2}$  with various input voltages under the working conditions that the output voltage is 50 V and the output power is 1-kW. From Fig. 12, it can be observed that: 1) the RMS values of  $i_{c1}$  and  $i_{c2}$  with the interleaving control strategy are much smaller than that without the interleaving control strategy; 2) the RMS values of  $i_{c1}$  and  $i_{c2}$  without the interleaving control strategy are different, contrarily the RMS values of  $i_{c1}$  and  $i_{c2}$  become almost the same by utilizing the interleaving control strategy; 3) without the interleaving control strategy, the RMS value of  $i_{c1}$  increases and the RMS value of  $i_{c2}$  decreases with the input voltage increasing, so the difference between these two RMS values would increase with the input voltage increasing. Contrarily, with the interleaving control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are kept almost same and constant with the

input voltage increasing because combining the proposed IPOP TL circuit structure and the interleaving control strategy can counteract part of the ripple currents on the two input capacitors; 4) the variation trends of the RMS values of  $i_{c1}$  and  $i_{c2}$  with the input voltage increasing are consistent with the theoretical analysis in the Section III-D; 5) the deviations between the experimental results and theoretical calculation results are very small, in which the biggest deviation is 0.29 A when the input voltage increases to 550 V. Such deviations are mainly caused by: 1) the output filter inductors are not large enough to be considered as current sources; 2) the input current cannot be considered as a constant; 3) there are minor differences between the circuit parameters of the two HB TL DC/DC converters; 4) there are some measurement errors especially for the small value measuring.

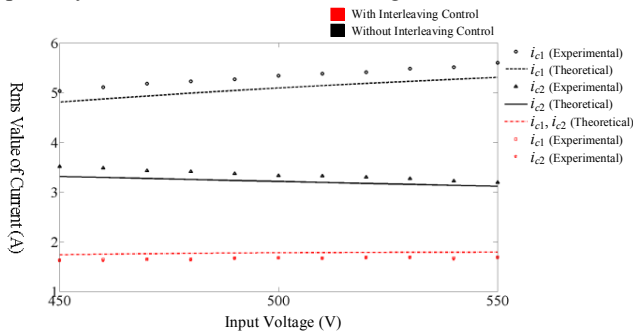


Fig. 12. RMS values of  $i_{c1}$  and  $i_{c2}$  with various input voltages under 1-kW. Note that “Experimental” and “Theoretical” in the legend indicate results through experiments and theoretical calculation, respectively.

The measured efficiency curves with respect to various input voltages are figured in Fig. 13. The peak efficiency with the interleaving control strategy is over 95%. By utilizing the interleaving control strategy, the ripple currents through the input capacitors can be largely reduced as shown in Fig. 2, which would reduce the power losses of the input capacitors and thus improve the efficiency of the converters in comparison with that without the interleaving control strategy as shown in Fig. 13.

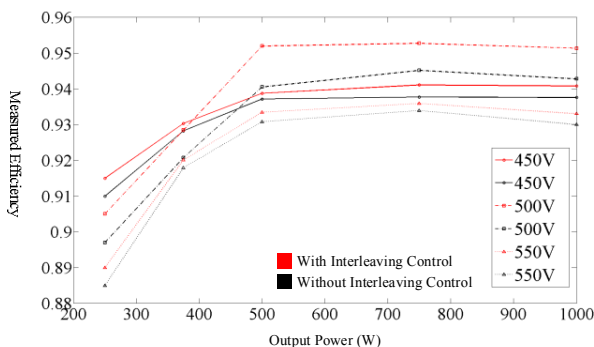


Fig. 13. Measured efficiency curves with various input voltages.

## V. CONCLUSION

This paper proposes the IPOP TL DC/DC converters, which are composed of the two four-switch HB TL DC/DC converters featuring with simple and compact circuit structure and associated with the interleaving control strategy, for

minimizing and balancing the capacitor ripple currents. Due to the combination of the proposed IPOP TL circuit structure and the interleaving control strategy, the ripple currents on the two input capacitors can be largely reduced not only by doubling the frequencies of these ripple currents as the universal benefit of using the interleaving control strategy but also by counteracting part of these ripple currents because of the operation principle of the proposed converters. In addition, the ripple current imbalance among the two input capacitors can be effectively eliminated by combining the proposed IPOP TL circuit structure and the interleaving control strategy. Therefore, the proposed converters with the interleaving control strategy can significantly improve the converter's performances in aspects of minimizing the size of the input capacitors, balancing the thermal stresses of the input capacitors, prolonging the lifetime of the input capacitors, and improving the reliability of the converter. Finally, the effectiveness and feasibility of the proposed IPOP TL converters with the interleaving control strategy are validated by the extensive theoretical analysis and the results obtained from simulation and experiments.

## APPENDIX

TABLE II  
PARAMETERS OF THE SIMULATION MODEL AND  
EXPERIMENTAL PROTOTYPE

Description	Parameter
Turns Ratios of $T_{r1}$ and $T_{r2}$	38 : 13
Leakage Inductances $L_{r1}$ and $L_{r2}$ (uH)	30
Output Filter Capacitor $C_o$ (uF)	470
Output Filter Inductors $L_{o1}$ and $L_{o2}$ (uH)	100
Input Capacitors $C_1$ and $C_2$ (uF)	14.4
DC-blocking Capacitors $C_{b1}$ and $C_{b2}$ (uF)	6
Switching Frequency (kHz)	50
Dead Time (ns)	400

## REFERENCES

- [1] R. S. Balog, W. Weaver, and P. T. Krein, “The load as an energy asset in a distributed DC smart grid architecture,” *IEEE Trans. Smart Grid*, vol. 3, no. 1, pp. 253–260, Mar. 2012.
- [2] H. Mohsenian-Rad, and A. Davoudi, “Towards building an optimal demand response framework for DC distribution networks,” *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2626–2634, Sep. 2014.
- [3] G. F. Reed, B. M. Grainger, A. R. Sparacino, and M. Zhi-Hong, “Ship to grid: Medium-voltage DC concepts in theory and practice,” *IEEE Power Energy Mag.*, vol. 10, no. 6, pp. 70–79, Nov. 2012.
- [4] K. Strunz, E. Abbasi, and D. N. Huu, “DC microgrid for wind and solar power integration,” *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 115–126, Mar. 2014.
- [5] S. Rodrigues, R. T. Pinto, P. Bauer, and J. Pierik, “Optimal power flow control of VSC-based multiterminal DC network for offshore wind integration in the North Sea,” *IEEE J. Emerging. Sel. Topics Power Electron.*, vol. 1, no. 4, pp. 260–268, Dec. 2013.
- [6] D. Boroyevich, I. Cvetkovic, R. Burgos, and D. Dong, “Intergrid: A future electronic energy network,” *IEEE J. Emerging. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 127–138, Sep. 2013.
- [7] S. Anand and B. G. Fernandes, “Optimal voltage level for DC microgrids,” in *Proc. IEEE Conf. Ind. Electron.*, 2010, pp. 3034–3039.
- [8] D. Salomonsson, L. Soder, and A. Sannino, “An adaptive control system for a DC microgrid for data centers,” *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1910–1917, Nov./Dec. 2008.
- [9] S. P. Engel, N. Soltau, H. Stagge, and R. W. De Doncker, “Improved instantaneous current control for high-power three-phase dual-active bridge DC–DC converters,” *IEEE Trans. Power. Electron.*, vol. 29, no. 8, pp. 4067–4077, Aug. 2014.



- [10] H. Sheng, F. Wang, and C.W. Tipton, "A fault-detection and protection scheme for three-level dc-dc converters based on monitoring flying capacitor voltage," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 685–697, Feb. 2012.
- [11] D. Liu, F. Deng, and Z. Chen, "Five-level active-neutral-point-clamped DC/DC converter for medium voltage DC grids," *IEEE Trans. Power Electron.*, to be published.
- [12] Y. Chen, M. Haj-ahmed, and M. S. Illindala, "An MVDC microgrid for a remote area mine site: Protection, operation and control," in *Proc. IEEE IAS Annu. Meet.*, Oct. 2014, pp. 1–9.
- [13] B. M. Grainger, A. R. Sparacino, R. J. Kerestes, and M. J. Korytowski, "Advancements in medium voltage DC architecture development with applications for powering electric vehicle charging stations," in *Energytech, 2012 IEEE*, 2012, pp. 1–8.
- [14] M. Saeedifard, M. Graovac, R. F. Dias, and R. Iravani, "DC power systems: Challenges and opportunities," in *Proc. IEEE Power Energy Soc. Gen. Meet.*, 2010, pp. 1–7.
- [15] J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter—a new concept in high-voltage DC-to-DC conversion," in *Proc. IEEE Int. Conf. Ind. Electron. Control Instrum. Autom.*, 1992, pp. 173–178.
- [16] F. Canales, P. Barbosa, M. Burdío, and F. Lee, "A zero-voltage switching three-level DC/DC converter," in *Proc. 22nd Int. Telecommun. Energy Conf.*, 2000, pp. 512–517.
- [17] F. Canales, P. Barbosa, and F. C. Lee, "A zero-voltage and zero-current switching three-level dc/dc converter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 898–904, Nov. 2002.
- [18] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC/DC converter: Four switches  $V_{pk} = V_{in}/2$ , capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 918–927, Jul. 2004.
- [19] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 395–404, Mar. 2005.
- [20] Z. Zhang and X. Ruan, "ZVS PWM full-bridge three-level converter," in *Proc. 4th Int. Power Electron. Motion Control Conf.*, 2004, pp. 1085–1090.
- [21] F. Deng and Z. Chen, "Control of improved full-bridge three-level DC/DC converter for wind turbines in a DC grid," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 314–324, Jan. 2013.
- [22] Y. Shi and X. Yang, "Soft switching PWM cascaded three-level combined DC–DC converters with reduced filter size and wide ZVS load range," *IEEE Trans. Ind. Electron.*, vol. 30, no. 12, pp. 6604–6616, Dec. 2015.
- [23] D. Kim, J. Kim, and G. Moon, "A three-level converter with reduced filter size using two transformers and flying capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 2140–2150, Jan. 2013.
- [24] B. Lin, and S. Chung, "New parallel ZVS converter with less active switches and smaller output inductance," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3297–3307, July. 2014.
- [25] Y. Shi, and X. Yang, "Wide-range soft-switching PWM three-level combined DC–DC converter without added primary clamping devices," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5157–5171, Oct. 2014.
- [26] B. Lin, and P. Cheng, "New ZVS DC–DC converter with series-connected transformers to balance the output currents," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 246–255, Jan. 2014.
- [27] Z. Guo, D. Sha, and X. Liao, "Hybrid phase-shift-controlled three-level and LLC DC–DC converter with active connection at the secondary side," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2985–2996, Jun. 2015.
- [28] Z. Guo, D. Sha, and X. Liao, "Hybrid three-level and half-bridge DC–DC converter with reduced circulating loss and output filter inductance," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6628–6638, Dec. 2015.
- [29] W. Li, S. Zong, F. Liu, H. Yang, X. He, and B. Wu, "Secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain for high input voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5128–5139, Nov. 2013.
- [30] D. Liu, F. Deng, Z. Gong, and Z. Chen, "A double phase-shift control strategy for a full-bridge three-level DC/DC converter," in *Proc. IECON*, Florence, Italy, Oct. 2016, pp. 1202–1207.
- [31] S. Yang *et al.*, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.
- [32] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.
- [33] C. Chang and M. A. Knights, "Interleaving technique in distributed power conversion systems," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 42, no. 5, pp. 245–251, May 1995.
- [34] R. Giral, L. Martinez-Salamero, and S. Singer, "Interleaved converters operation based on CMC," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 643–652, Jul. 1999.
- [35] H. Hao, G. A. Covic, and J. T. Boys, "A parallel topology for inductive power transfer power supplies," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1140–1151, Mar. 2014.
- [36] J. Shi, L. Zhou, and X. He, "Common-duty-ratio control of input-parallel output-parallel (IPOP) connected DC-DC converter modules with automatic sharing of currents," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3277–3291, Jul. 2012.



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